Introduction

Amplifiers with internal voltage clamps, also known as limiting amplifiers, have a wide range of practical uses. They are most commonly used to protect load circuitry that has a limited input range. By connecting the high and low clamp pins to DC levels, the output voltage may be restricted to the desired range. The internal clamp circuitry also avoids saturation of the output stage devices and assures fast overload recovery.

Prior to the introduction of limiting amplifiers, design engineers had to develop their own limiting networks. This network was as simple as two Schottky diodes and a current limiting resistor, or as complicated as an adjustable limiting network that might employ several transistors, resistors and diodes. With limiting amplifiers, adjustable limiting networks are realized with a simple resistor divider network connected to the high and/or low limit pins.

Many other applications exist for limiting amplifiers. Because of their fast response time and flexibility in output voltage range, they make excellent high performance comparators. Several applications make use of the wide bandwidth of the clamp inputs. Through appropriate modulation of the clamp input voltages, an AM modulator, soft clipping circuit and sync stripper can be realized. This application note describes how amplifiers with internal clamps work, the advantages of using these amplifiers for limiting and a number of application circuits.

Input vs Output Limiting

There are two classes of limiting amplifiers on the market today, those that employ input limiting to constrain the output voltage, and those that utilize output limiting. Each has their own advantages, and users should understand these issues and pick the best one for their application. Advantages of input limiting amplifiers include: better clamp accuracy, continued low closed loop output impedance during limiting, and depending on the implementation, input limiting may or may not prevent input stage saturation.

Input limiting amplifiers have some serious limitations, however, which are not shared by output limiting versions. The input limiting amplifier offers no limiting action when configured in inverting gains, and does not protect against transients introduced at the inverting input, because the input limiting function applies only to the positive input.

Additionally, because the limiting voltages are applied to the input stage, they are amplified by the op amp's gain. This precludes the use of input limiting amps in open loop configurations (e.g., comparators) and makes the setting of the limit voltages much more critical. Consider a limiting amplifier in a closed loop gain of 10. A 10mV error in setting the limit voltage translates into a 100mV error at the output of an input limiting amplifier, while the output limiting amp

delivers only the 10mV error. If an input limiting amplifier becomes damaged and goes open loop, the rail-to-rail output swing will likely take out the expensive A/D it was designed to protect. Output limiting controls the output excursions as long as the limiting circuitry remains functional. This application note focuses on output limiting amplifiers due to their greater flexibility.

Output Limiting Current Feedback Amplifiers

Intersil's line of output limiting amplifiers are current feedback op amps which feature user programmable output clamps to limit output voltage excursions. Limiting action is obtained by applying voltages to the V_H and V_L terminals (pins 8 and 5) of the amplifier. V_H sets the upper output limit, while V_L sets the lower clamp level. If the amplifier tries to drive the output above V_H, or below V_L, the clamp circuitry limits the output voltage at V_H, or V_L ($\pm$ the clamp accuracy) respectively. The output voltage remains at the clamp level as long as the overdrive condition remains.

When the input voltage drops below the overdrive level (V_{CLAMP} / A_{VCL}) the amplifier returns to linear operation. A time delay, known as the Overdrive Recovery Time, is required for this resumption of linear operation. The clamped overdrive recovery time may be an order of magnitude faster than the amplifier's normal saturation recovery time. The low input bias currents of the clamp pins allow them to be driven by simple resistive divider circuits, or active elements such as amplifiers or D/A converters. Because the clamp circuit is part of the amplifier, and the amp has been characterized with the clamp circuit present, the user can be confident that the clamp circuitry will induce minimal performance degradation during normal linear operation.

Clamp Circuitry

Figure 1 shows a simplified schematic of the HFA1130 input stage, and the high clamp (V_H) circuitry. As with all current feedback amplifiers, there is a unity gain buffer (Q_{X1} - Q_{X2}) between the positive and negative inputs. This buffer forces -IN to track +IN, and sets up a slewing current equal to the current flowing through the inverting input. This current is mirrored onto the high impedance node (Z) by Q_{X3} - Q_{X4}, where it is converted to a voltage and fed to the output via another unity gain buffer. If no clamping is utilized, the high impedance node may swing within the limits defined by Q_{P4} and Q_{N4}. Note that when the output reaches its quiescent value, the current flowing through -IN is reduced to only that small current ($-I_{BIAS}$) required to keep the output at the final voltage.
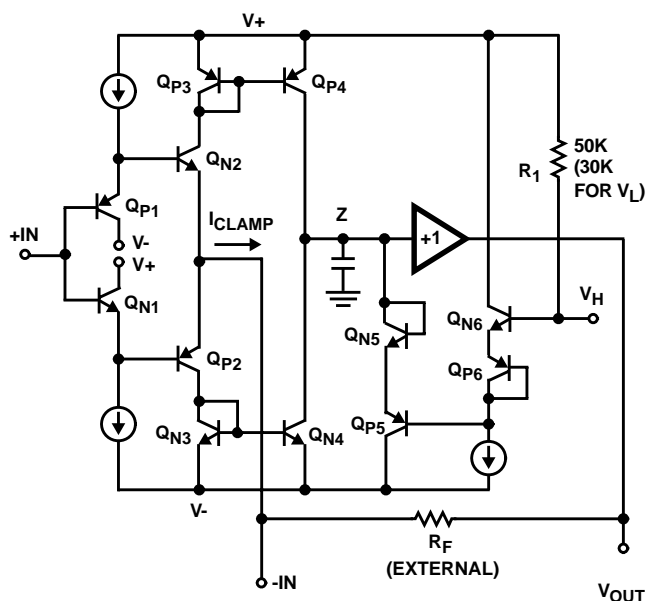
FIGURE 1. HFA1130 SIMPLIFIED V_H CLAMP CIRCUITRY

Tracing the path from node V_H to node Z illustrates the effect of the clamp voltage on the high impedance node. V_H decreases by $2V_{BE}$ (Q_{N6} and Q_{P6}) to set up the base voltage on Q_{P5}. Q_{P5} begins to conduct whenever the high impedance node reaches a voltage equal to Q_{P5}'s base + $2V_{BE}$ (Q_{P5} and Q_{N5}). Thus, Q_{P5} clamps node Z whenever Z reaches V_H. R_1 provides a pull-up network to ensure functionality with the clamp input floating. A similar description applies to the symmetrical low clamp circuitry controlled by V_L.

When the output is clamped, the negative input continues to source a slewing current (I_{CLAMP}) in an attempt to force the output to the quiescent voltage defined by the input. Q_{P5} must sink this current while clamping, because the -IN current is always mirrored onto the high impedance node.

Clamp Accuracy

The clamped output voltage will not be exactly equal to the voltage applied to V_H or V_L. Offset errors, mostly due to V_{BE} mismatches, cause inaccuracies in the clamping level. Clamp accuracy is a function of the clamping conditions. Referring again to Figure 1, it can be seen that one component of clamp accuracy is the V_{BE} mismatch between the Q_{X6} transistors, and the Q_{X5} transistors. If the transistors are run at the same current level there is no V_{BE} mismatch, and no contribution to the inaccuracy. The Q_{X6} transistors are biased at a constant current, but as described earlier, the current through Q_{X5} is equivalent to I_{CLAMP}. V_{BE} increases as I_{CLAMP} increases, causing the clamped output voltage to increase as well. I_{CLAMP} is a function of the overdrive level and R_F, so clamp accuracy degrades as the overdrive increases, and as R_F decreases. Consideration must also be given to the fact that the clamp voltages have an effect on amplifier linearity. As the output voltage approaches the clamp level the clamp circuitry starts to conduct and linearity degrades. Most limiting

amplifier data sheets detail the impact on linearity in a graph entitled: "Non-linearity Near Clamp Voltage".

Clamp Range

Unlike some limiting amplifiers, both V_H and V_L of HFA series amplifiers have usable ranges that cross 0V. While V_H must be more positive than V_L, both may be positive or negative, within the range restrictions indicated in the specifications. For example, the HFA1130 output could be limited to ECL levels by setting V_H = -0.8V and V_L = -1.8V.

Use as a Protection Circuit

Limiting amplifiers are frequently used to protect circuitry that has a limited input range. A classic example is a buffer for an A/D converter. Many A/D converters can be damaged if their input is taken much beyond their specified input range. In addition to providing necessary input voltage clamping, a limiting amplifier can provide the peak currents needed to charge the A/D converter input capacitance and remain stable with step changes in input voltage. Of course, the limiting amplifier can also provide the gain and level shifting frequently required preceding an A/D converter.

In Figure 2, the HFA1135 limiting amplifier is used to drive the HI1175 8-bit, 20 MSPS A/D Converter. The HFA1135 is configured as a level shifting amplifier with an offset of 0.5V and a gain of 2. This allows a ground referenced, 1V Max signal to span the full 2V input range of the HI1175. The HI1175 is typical of many single supply A/D converters which have an input range that does not include ground. The V_{RT} and V_{RB} voltages of 2.5V and 0.5V respectively set the limits of the HI1175 input range. The V_L clamp voltage of 0V keeps the lower limit of the input to the HI1175 within its absolute maximum range. The 0.5V difference between the nominal minimum input voltage and the clamp voltage assures that the clamp circuitry does not effect the linearity of the circuit. A voltage divider sets the V_H voltage to approximately 3V.
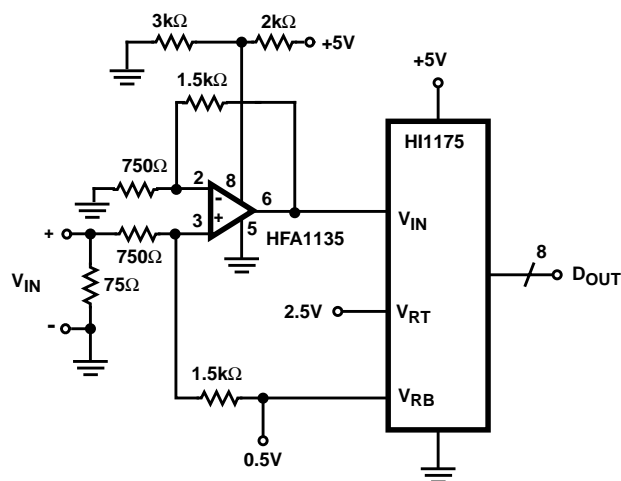

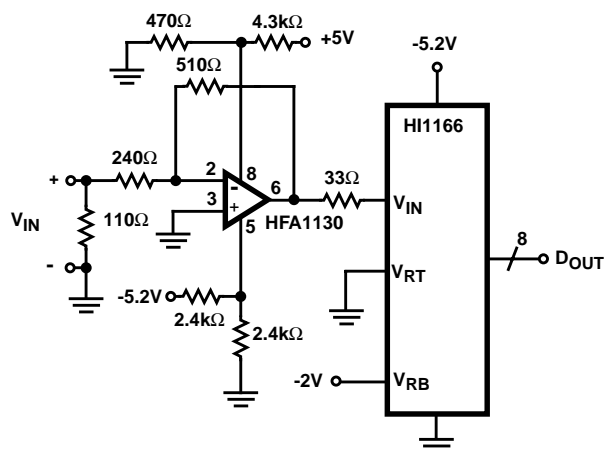**FIGURE 2. HFA1135 DRIVING THE HI1175 ADC**

FIGURE 3. HFA1130 DRIVING THE HI1166 ADC

In Figure 3, the HFA1130 is used in a gain of -2 to drive the input of the HI1166 8-bit, 250 MSPS A/D Converter. Typical of A/D converters that operate above 100Msps, the HI1166 is an ECL part that runs from power supplies of GND and -5.2V. The HFA1130 allows a 0V to 1V input to span the 0V to -2V range of the A/D converter. Resistor dividers set the V_H and V_L limit levels to 0.5V and -2.5V respectively.

Using Current Feedback Amplifiers as Comparators

Current feedback amplifiers, especially those with output limiting, make excellent high speed, open loop comparators. Recall that the non-inverting input connects to the input of a unity gain buffer, while the inverting input connects to the buffer output. This buffer sources or sinks current until the error current is minimized, and this buffer current is mirrored onto the high impedance node to provide the slewing current. Since the slewing current is proportional to the current flowing through the amplifier's inverting input, the slew rate may be adjusted by the external resistance on the inverting input.

If a voltage is applied to the non-inverting input, the internal buffer forces the inverting input to the same voltage, the buffer will sink or source current accordingly, and the amplifier output will fall or rise respectively. With no provision for feedback, the buffer's current remains constant, and the output drives into the stops resulting in output saturation with its undesirable effects.

Consider the HFA1130 based inverting comparator circuit (Figure 4). The GND at the HFA1130's non-inverting input forces the internal buffer to output 0V at the inverting input. As soon as V_{IN} rises above 0V, the input buffer begins sinking current, and the output signal falls to its negative stop. When V_{IN} returns below GND, the output transitions high.
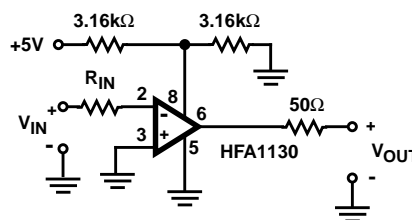

FIGURE 4. HFA1130 IMPLEMENTED AS AN INVERTING, 2ns, TTL COMPATIBLE OUTPUT COMPARATOR

Because of the HFA1130's relatively small propagation delay of 0.5ns, the dominant component of the comparator's response time is the op amp's slew rate. Since the slew rate is a function of I_{IN}, the response time is strongly influenced by V_{IN}, and the choice of R_{IN}. Decreasing R_{IN} decreases the response time, with a slight decrease in limiting accuracy, (Figure 5). However, if R_{IN} is too small the internal current mirrors can saturate and reverse the effect. To implement a non-inverting comparator, simply ground the outboard side of R_{IN}, and apply the input signal to the amplifier's non-inverting input.
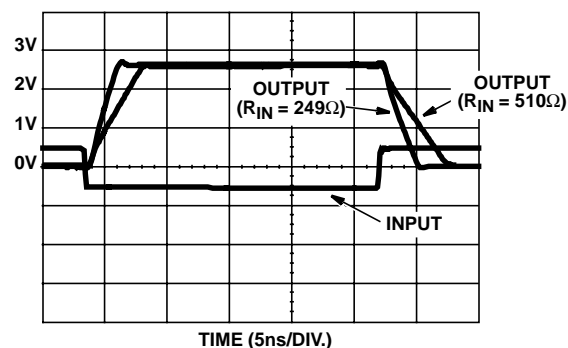

FIGURE 5. DECREASING R_{IN} REDUCES THE COMPARATOR RESPONSE TIME FROM 2.5ns TO 1.2ns

Comparator Benefits From Output Limiting

The HFA1130's open loop response plot (Figure 6) illustrates the key advantages of using output limiting amplifiers for comparator applications. Besides the obvious benefit of constraining the output swing to a defined logic range, limiting the output excursions also keeps the output transistors from saturating which prevents unwanted saturation artifacts from distorting the output signal. Utilizing the output limiting function also takes advantage of the HFA1130's ultra-fast recovery from clamped overdrive (<1ns). Instead of the >10ns propagation delay (the HFA1130's normal saturation recovery time) obtained with the unrestricted output, limiting the positive swing to 2.5V yields a 2ns response time.
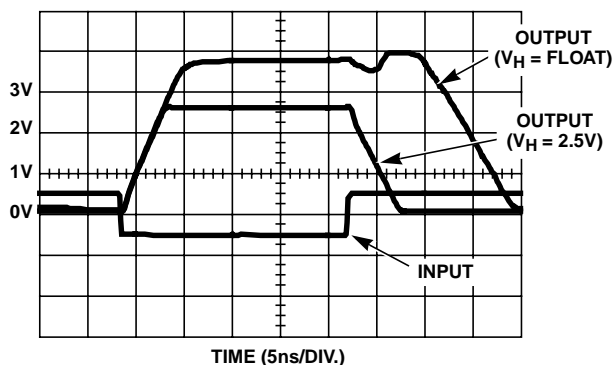
FIGURE 6. COMPARISON OF COMPARATOR RESPONSE WITH AND WITHOUT OUTPUT LIMITING

AM Modulator Circuit

The fast overdrive recovery time and wide bandwidth of the clamp inputs allows these inputs to be driven by high frequency AC as well as DC signals. When driven at the appropriate levels, the clamp inputs may be used to form an AM modulator. Figure 7 shows a complete AM modulator circuit. The HFA1130 Limiting Amplifier is driven by a $4V_{P-P}$ carrier signal. The gain of 2 through the HFA1130 insures that the carrier amplitude is sufficient to drive the output over its $\pm3.3V$ range.

FIGURE 7. AM MODULATOR UTILIZING THE HFA1130 LIMITING CAPABIILITY

The HFA1212 performs the necessary level shifting and inversion to convert the modulating signal input into a pair of anti-phase signals that control the high and low clamp inputs. U_{1A} inverts the signal and level shifts to -1.5V. U_{1B} inverts that signal forming a complimentary signal centered at +1.5V.

With a signal input of 0V, U_2 produces a $3V_{P-P}$ output at the carrier frequency. As the signal input varies, U_2 produces a symmetrically modulated carrier with a maximum amplitude of $6V_{P-P}$. The oscilloscope photograph in Figure 8 shows a 5MHz carrier AM modulated by a 100kHz signal. The $2300V/\mu s$ slew rate of the HFA1130 limits $6V_{P-P}$ amplitude

carrier signals to a frequency of 61MHz. If adjusted for lower output signal levels, the carrier and modulating frequencies can be increased to well above 100MHz.
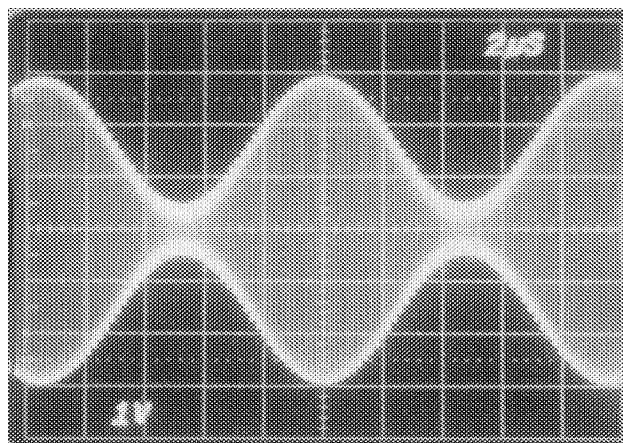

FIGURE 8. A 5MHz CARRIER IS AM MODULATED BY A 100kHz SIGNAL

Soft Clipping Circuit

Any amplifier stage driven to the limit of its linear range will cause signal clipping. The circuit described here establishes a clipping level that is a function of the input signal. The result is a soft clamp function where the amplifier has one gain in its linear operating range and a user programmable lower gain when the output reaches an arbitrary threshold. The circuit may be used in imaging applications to expand the contrast of low level signals. It can be used in audio circuits to avoid generation of objectionable harmonics due to hard clipping. It also has application in control loops that otherwise would become unstable when their error amplifiers saturate. This circuit can be used in a broad range of applications that require a combination of high sensitivity for low level signals and wide dynamic range.

The basic soft clipping circuit, based on the HFA1135, is shown in Figure 9. The nominal value of R_1 is 1.5kΩ which is the optimum feedback resistor for the HFA1135. Hard clamping results with R_2 and R_4 shorted, and R_3 and R_5 removed. Figure 10 illustrates the hard clamping operation with a 100kHz input signal and clamp levels set at $\pm1V$. The circuit has unity gain for inputs that fall between the clamp levels. The addition of R_2 through R_5 make the clamp level a function of the input signal. The output for signals in excess of V_{CH} (Voltage Clamp High) is given by:
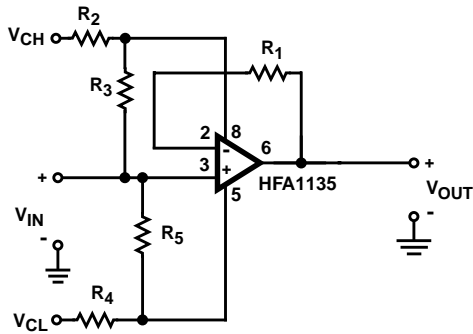
$$V_O = (V_{IN}R_2 + V_{CH}R_3) / (R_2 + R_3).$$

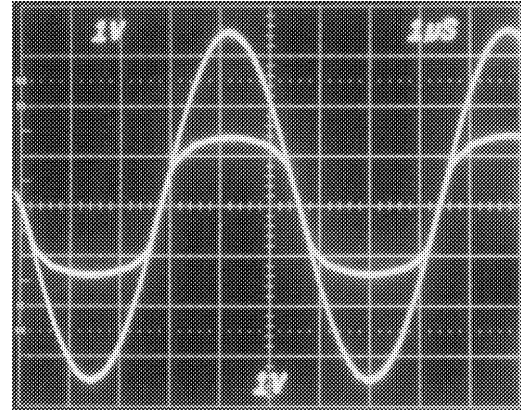**FIGURE 9. HFA1135 OUTPUT LIMITING AMPLIFIER CONFIGURED FOR SOFT LIMITING**

FIGURE 11. SOFT CLIPPING WITH A GAIN OF 1/6 ABOVE THE CLAMP LEVEL
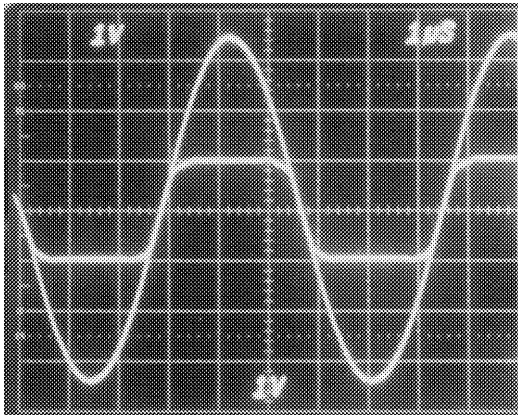

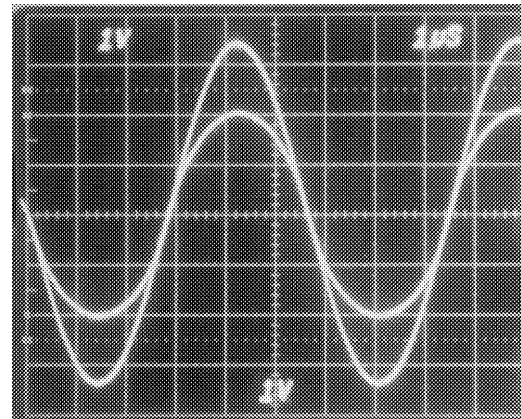**FIGURE 10. HARD CLIPPING RESULTS FROM A GAIN OF ZERO ABOVE THE CLAMP LEVEL**

FIGURE 12. SOFT CLIPPING WITH A GAIN OF 1/2 ABOVE THE CLAMP LEVEL

Figure 11 shows the result with R_2 and R_4 set to 1kΩ, and R_3 and R_5 set to 5kΩ. The gain for signals greater than 1V is 1/6. In Figure 12, R_2 through R_5 have been set to 1kΩ, and the gain above 1V is 1/2. Note that the high and low clamp levels need not be symmetrical, and the attenuation factors above and below those levels may be different.

Limiting amplifiers are frequently used at the front end of systems to accommodate wide dynamic range signals that may extend beyond the common mode range of the system.

While the circuit in Figure 9 performs soft clipping, it is restricted to signals within the ±2.4V input voltage range of the HFA1135. The circuit in Figure 13 incorporates an additional clamp network that allows the circuit to be used with signals that exceed the input voltage range. Using the values shown, the circuit has unity gain for signals that range between ±1V. The gain for inputs beyond that range is 1/6. Soft clipping works for signals up to ±9.4V which is well in excess of the ±5V power supply levels for the HFA1135.
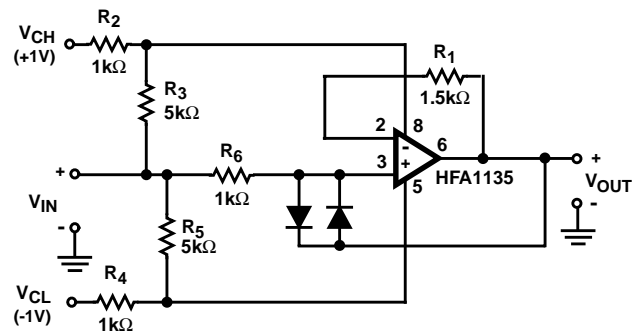

FIGURE 13. SOFT CLIPPING CIRCUIT WITH EXTENDED INPUT RANGE

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